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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,608	11/28/2003	Shigemi Yoshioka	OKI.269D2	8243

7590 04/27/2004

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,608	YOSHIOKA, SHIGEMI	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 20-38 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 20-38 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/962,442.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Pre-amendment filed on November 28, 2003 has been entered.

2. Claims 1-19 have been canceled.

3. Claims 20-38 have been added.

4. Claims 20-38 are presented for examination.

Priority

5. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/962,442, filed on 09/26/2001.

Information Disclosure Statement

6. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on December 28, 2003.

7. Information disclosed and list on PTO 1449 was considered.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 20, 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 20, the limitation "an input/output circuit selectively connected to the register". However, applicant does not reveal what register, because having two kinds of register is defined, one is write register, one is read register. Which one is claimed?

Claim is required to amend for more clearly.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 20-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwamoto et al. (U.S. Patent No. 5,592,434).

Regarding claims 20, 27,33, Iwamoto et al. disclose a serial access memory (Figure 2) comprising:

a first memory array (Figure 2, first column) including a plurality of first memory cells (MC) , a first sense amplifier (SA) and a pair of first bit lines (BL, /BL) connected to the first memory cells and the first sense amplifier;

a second memory array (Figure 2, BLP) including a plurality of second memory cells (MC), a second sense amplifier SA) and a pair of second bit lines (BLP) connected to the second memory cells and the second sense amplifier;

a pair of column lines (Figure 2, CSL, CSL') selectively connected to the first bit lines or the second bit lines, the column lines being located substantially parallel with the first and second bit lines (Figure 2, CSL, CSL' parallel BL, /BL) ;

a write register connected to the column lines (Figure 1, 59);

a read register connected to the column lines (Figure 1, 56);

a control circuit (Figure 2, transistors connected between BL and CSL, and /BL and CSL') selectively connecting the column lines with the first bit lines or the second bit lines;

an input/output circuit selectively connected to the registers (Figure 1, 57, 58) .

Regarding claims 21-26, 28-32, 34-38, Iwamoto et al. disclose wherein the input/output circuit includes an input circuit (Figure 14, 37a) selectively connected to the write register and an output circuit (Figure 14, 32a) selectively connected to the read register, and Iwamoto et al. disclose an additional read register (Figure 1, 56b) connected to the column lines and an additional output circuit (Figure 1, 57b) connected to the additional read register, and wherein the control circuit (Figure 2, CSG2) comprises a first transfer circuit connected between the column lines and the first bit lines (Figure 2, transistor coupled between BL, /BL and CSL, CSL'), the first transfer circuit connecting the column lines with the first bit lines in response to a first control signal (Figure 3, signal from CDU); and a second transfer circuit (figure 2, transistor coupled BLP) connected between the column lines and the second bit lines, the second transfer circuit connecting the column lines with the second bit lines in response to a second control signal (Figure 3, Φ A1), and a third transfer circuit (Figure 1, 2a)

connected between the column lines and the read register ,the third transfer circuit connecting the column lines with the read registers in response to a third control signal (Figure 1, ΦPA1) ; and a fourth transfer circuit (Figure 1, ΦRr1) connected between the read register and the input/output circuit, the fourth transfer circuit connecting the read register with the input/output circuit in response to a fourth control signal (Figure 1, ΦOE1), and a fifth transfer circuit (Figure 1, 3a) connected between the column lines and the write register, the fifth transfer circuit connecting the column lines with the write register in response to a fifth control signal (Figure 1, Φ WB1), and a sixth transfer circuit connected between the write register and the input/output circuit, the sixth transfer circuit connecting the write register with the input/output circuit in response to a sixth control signal (Figure 1, Φ DB1), and wherein the read register is selectively connected to two pairs of column lines, and the write register is selectively connected to the two pairs of column lines (Figure 4, two pairs of column lines are GIOL'/GIOL', GIOL, /GIOL).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER